REMARKS

Claims 1-4, 6-11, 13, 14 and 16-20 are pending in the present application. Claims 1, 3, 4, 7-11, 14, 16 and 19 have been amended. Claims 5, 12 and 15 have been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Claim Rejections-35 U.S.C. 112

Claim 4 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 4 has been amended to feature that the dielectric layer "is substantially coplanar and aligned with a top surface of the second region", to be in better compliance with 35 U.S.C. 112, second paragraph. The Examiner is therefore respectfully requested to withdraw this rejection.

Claim Rejections-35 U.S.C. 102

Claims 1-3, 5-10 and 13-15 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Basceri et al. reference (U.S. Patent No. 6,444,478). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The ferroelectric capacitor of claim 1 includes in combination a bottom electrode "which has a first region and a second region, wherein the first region has a first thickness and the second region has a second thickness greater than the first thickness, and wherein the second region is arranged at a central area of the bottom electrode and the first region is arranged at a peripheral area of the bottom electrode"; a dielectric layer; a ferroelectric layer; and a top electrode, "wherein the dielectric layer sandwiched between the first region of the bottom electrode and the ferroelectric layer, and wherein a side surface of the first region of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned". Applicant respectfully submits that the Basceri et al. reference as relied upon by the Examiner does not disclose these features.

Applicant respectfully submits that bottom electrode 32 as illustrated in Fig. 2 of the Basceri et al. reference is planar, and is not disclosed or even remotely suggested as having first and second regions of different thickness, and wherein the first and second regions of different thickness are arranged respectively at peripheral and central areas of the bottom electrode. Electrode 32 is described in column 14, lines 14-20 of the Basceri et al. reference as generally formed from one or more layers or films of various materials. However, there is no specific teaching or suggestion that electrode 32 of the Basceri et al. reference has regions of different thickness. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 1 distinguishes over the Basceri et al. reference as relied upon by the Examiner, and that this rejection, insofar

as it may pertain to claims 1-3 and 6-9, is improper for at least these reasons.

The ferroelectric capacitor of claim 10 includes in combination a bottom electrode "having a step area"; a top electrode; a ferroelectric layer; and a dielectric spacer, "wherein a distance between the bottom electrode and the top electrode at the step area is greater than a distance between the bottom electrode and the top electrode at a central area of the ferroelectric capacitor, and wherein the dielectric spacer decreases an electric field strength at the step area of the bottom electrode".

As emphasized above, bottom electrode 32 in Fig. 2 of the Basceri et al. reference is depicted as planar in nature, and generally described as formed of various different layers. Bottom electrode 32 in Fig. 2 of the Basceri et al. reference is not described or even remotely suggested as having a step area, so that a distance between a bottom electrode and a top electrode at the step area is greater than a distance between the bottom electrode and the top electrode at a central area of the capacitor. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 10 distinguishes over the Basceri et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 10 and 13, is improper for at least these reasons.

The ferroelectric capacitor of claim 14 includes in combination a first electrode; a spacer layer "formed on a peripheral area of the first electrode and arranged around the projecting portion of the first electrode"; a ferroelectric layer; and a second electrode, "wherein a side surface of the plate portion of the first electrode, a side surface of the

ferroelectric layer and a side surface of the second electrode are aligned".

The Examiner has interpreted interfacial layer 14 of dielectric film 12 as illustrated in Fig. 1 of the Basceri et al. reference as the spacer layer of claim 14. Dielectric film 34 in Fig. 2 of the Basceri et al. reference would correspond to dielectric film 12 in Fig. 1 thereof. Since dielectric film 34 in Fig. 2 of the Basceri et al. reference is merely formed on bottom electrode 32, a corresponding interfacial layer of dielectric film 34 in Fig. 2 of the Basceri et al. reference is not **arranged around** a projecting portion of a first electrode, as would be necessary to meet the features of claim 14. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 14 distinguishes over the Basceri et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 14, is improper for at least these reasons.

Claims 1, 4, 11 and 12 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Natori et al. reference (U.S. Patent No. 6,459,111). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Applicant initially notes that grouping of dependent claims 11 and 12 in this rejection is improper, because base claim 10 is not included. **The Examiner is therefore respectfully requested to withdraw this rejection insofar as it may pertain to claims 11 and 12.**

The Examiner has interpreted lower electrode 39, insulating film 40, ferroelectric

layer 42 and upper electrode 43 in Fig. 3 of the Natori et al. reference respectively as the bottom electrode, the dielectric layer, the ferroelectric layer and the top electrode of claim 1. However, the side surfaces of lower electrode 39, insulating film 40, ferroelectric layer 42 and upper electrode 43 in Fig. 3 of the Natori et al. reference are not aligned, as would be necessary to meet the features of claim 1. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 1 distinguishes over the Natori et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1 and 4, is improper for at least these reasons.

As noted above, claim 10 has not been rejected under 35 U.S.C. 102(e) as being anticipated by the Natori et al. reference. Applicant however respectfully emphasizes that lower electrode 39 in Fig. 3 of the Natori et al. reference is not disclosed as including a step area and the distances as featured in claim 10.

Claim Rejections-35 U.S.C. 103

Claims 16-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Natori et al. reference in view of the Eguchi reference (U.S. Patent No. 6,093,575). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 16 includes in combination a semiconductor substrate; a switching transistor; an insulating layer; a ferroelectric capacitor; and a plug electrode. The ferroelectric capacitor includes features somewhat similar as set forth in

claim 1.

Applicant respectfully submits that the Eguchi reference as relied upon by the Examiner does not overcome the previously noted deficiencies of the Natori et al. reference as described with respect to claim 1. Particularly, the Eguchi reference would provide no motivation to modify the structure in Fig. 3 of the Natori et al. reference to include aligned side surfaces as featured in claim 16. Applicant therefore respectfully submits that the semiconductor device of claim 16 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 16-18, is improper for at least these reasons.

Claims 19 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Natori et al. reference in view of the Kobayashi reference (U.S. Patent No. 6,495,879). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 19 includes in combination a semiconductor substrate; a switching transistor; an insulating layer; a ferroelectric capacitor; and a wiring. The ferroelectric capacitor is featured in a somewhat similar manner as in claim 1.

Applicant respectfully submits that the Kobayashi reference as relied upon by the Examiner does not overcome the above noted deficiencies of the Natori et al. reference as described with respect to claim 1. Particularly, the Kobayashi reference would

provide no motivation to modify the Fig. 3 structure of the Natori et al. reference to have side surfaces that are aligned, as featured in claim 19. Applicant therefore respectfully submits that the semiconductor device of claim 19 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 19 and 20, is improper for at least these reasons.

Conclusion

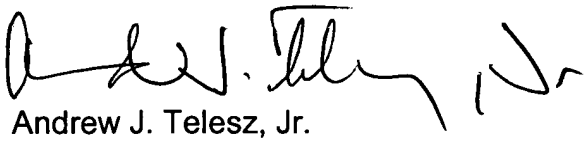
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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